Electronic Version
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Claims

[c1] 1.A Universal-Serial-Bus (USB) single-chip flash device comprising:

a USB flash microcontroller having a central processing unit (CPU) for executing instructions and a random-access memory (RAM) for storing instructions for execution by the CPU;

a serial engine in the USB flash microcontroller for receiving USB packets from a host over a host USB bus;

a flash-memory controller in the USB flash microcontroller;

flash mass storage blocks, coupled to the flash-memory controller, for storing non-volatile data for the host, the data in the flash mass storage blocks being block-addressable and not randomly-addressable; and

a flash bus having parallel data lines for transferring data from the flash-memory controller to the flash mass storage blocks, the flash bus also carrying a command to the flash mass storage blocks over the parallel data lines and also carrying a flash address over the parallel data lines;

wherein a block of data in the flash mass storage blocks is addressable by the flash-memory controller sending the command and a physical address over the parallel

data lines, the command and the physical address being used to transfer the block of data over the parallel data lines as a plurality of data words transferred in a plurality of bus cycles;

whereby the USB flash microcontroller is integrated with the flash mass storage blocks that are block-addressable.

[c2] 2.The USB single-chip flash device of claim 1 wherein instructions are stored only in the RAM for execution, wherein the CPU executes instructions stored only in the RAM;

wherein the instructions are transferred from a copy of the instructions in the flash mass storage blocks to the RAM during a power-on sequence before the CPU;

whereby instructions are transferred from the flash mass storage blocks to the RAM for execution by the CPU.

[c3] 3.The USB single-chip flash device of claim 2 wherein the USB flash microcontroller does not contain a read-only memory (ROM) for storing instructions that is directly addressable by the CPU.

[c4] 4.The USB single-chip flash device of claim 2 wherein the flash mass storage blocks output instructions stored in a first page during the power-up sequence before the command or the physical address have been sent over

the parallel data lines to the flash mass storage blocks, whereby the flash mass storage blocks automatically read instructions stored in the first page during the power-on sequence.

[c5] 5.The USB single-chip flash device of claim 4 further comprising:
a direct-memory access (DMA) engine for transferring data among the flash-memory controller, the RAM, and the serial engine, the DMA engine being programmed for a transfer.

[c6] 6.The USB single-chip flash device of claim 5 further comprising:
a flash programming engine, coupled to the flash-memory controller, for programming the DMA engine to transfer instructions from the first page of the flash mass storage blocks to the RAM during an initial portion of the power-on sequence.

[c7] 7.The USB single-chip flash device of claim 6 wherein the instructions transferred from the first page of the flash mass storage blocks comprise a boot loader program;
wherein the CPU is brought out of reset and begins executing instructions from the RAM once the boot loader program has been transferred to the RAM by the DMA engine;

wherein the CPU executes the boot loader program loaded into the RAM from the flash mass storage blocks.

[c8] 8.The USB single-chip flash device of claim 7 wherein the boot loader program contains instructions for the CPU to transfer a control program from the flash mass storage blocks to the RAM, the control program being executed by the CPU upon completion of transfer.

[c9] 9.The USB single-chip flash device of claim 2 wherein the USB single-chip flash device has only two data pins, the two data pins being a pair of differential serial data lines for transferring serial USB data over the host USB bus.

[c10] 10.The USB single-chip flash device of claim 9 wherein the USB single-chip flash device is in a package having ten or fewer external pins.

[c11] 11.The USB single-chip flash device of claim 2 wherein the physical address is a partial address of a page of data in the flash mass storage blocks, the partial address having fewer address bits than a full word address that uniquely identifies a word of data in the flash mass storage blocks that can be transferred over the parallel data lines in a single bus cycle.

[c12] 12.The USB single-chip flash device of claim 2 further comprising:

an internal bus in the USB flash microcontroller, the internal bus connecting to the CPU, to the RAM, to a buffer for the serial engine, and to the flash-memory controller;

wherein the instructions executed by the CPU are transferred from the flash mass storage blocks over the flash bus to the flash-memory controller and then to the internal bus for storage by the RAM.

[c13] 13.A ROM-less single-chip flash device comprising:

a serial interface to a serial-data bus that connects to a host;

a serial engine for detecting and processing packets sent over the serial-data bus;

a serial-engine buffer for storing data sent over the serial-data bus;

an internal bus coupled to the serial-engine buffer;

a random-access memory (RAM) for storing instructions for execution, the RAM on the internal bus;

a central processing unit, on the internal bus, the CPU accessing and executing instructions in the RAM;

a flash-memory controller, on the internal bus, for generating flash-control signals and for buffering commands, addresses, and data to a flash bus;

flash mass storage blocks coupled to the flash-memory controller by the flash bus, and controlled by the flash-control signals;

a direct-memory access (DMA) engine, on the internal bus, for transferring data over the internal bus; and

a flash programming engine, activated by a reset, for initially programming the DMA engine to transfer an initial program of instructions from the flash mass storage blocks to the RAM before the CPU begins execution of instructions after the reset;

whereby the initial program of instructions is transferred from the flash mass storage blocks to the RAM before execution by the CPU begins, eliminating a need for a local read-only memory (ROM) for storing the initial program of instructions.

[c14] 14.The ROM-less single-chip flash device of claim 13 wherein the initial program of instructions is a boot-loader program that programs transfers a control program of instructors from the flash mass storage blocks to the RAM when the CPU begins execution of the boot-loader program after reset.

[c15] 15.The ROM-less single-chip flash device of claim 14 wherein data in the flash mass storage blocks are accessible by the flash-memory controller sending a request sequence over the flash bus, the request sequence including a command followed by a physical address;

wherein the data in the flash mass storage blocks is block-addressable while the RAM is randomly-ad-

dressable by the CPU.

[c16] 16.The ROM-less single-chip flash device of claim 15 wherein the flash mass storage blocks are initially readable after a reset before receiving a command and a physical address over the flash bus;
wherein the flash mass storage blocks send data in a first page over the flash bus after the reset and before receiving a command and a physical address over the flash bus.

[c17] 17.The ROM-less single-chip flash device of claim 13 wherein the ROM-less single-chip flash device is one of a plurality of ROM-less single-chip flash device that are connected to a USB switch by a plurality of serial-bus segments;
wherein the USB switch aggregates flash storage capacity of the plurality of ROM-less single-chip flash devices and reports to the host as a single endpoint of the host.

[c18] 18.The ROM-less single-chip flash device of claim 17 wherein the USB switch re-orders packets from the host.

[c19] 19.A flash drive comprising:
a switch that connects to a host over a host bus, and connects to downstream devices over a plurality of serial buses;

a plurality of serial single-chip flash devices, coupled to the switch as the downstream devices, each serial single-chip flash device comprising:
a serial-flash microcontroller having a processor;
a main memory coupled to the processor for storing instructions for execution by the processor;
a serial interface the switch through one of the plurality of serial buses;
a flash-memory controller;
a plurality of flash mass storage blocks that are block-accessible by the CPU through the flash-memory controller;
a direct-memory access (DMA) engine for directly transferring data and instructions over an internal bus among the serial interface, the main memory, the CPU, and the flash-memory controller;
a flash programming engine for initially programming the DMA engine to read an initial program from first page of the plurality of flash mass storage blocks and write the initial program to the main memory for execution by the CPU.

[c20] 20.The flash drive of claim 19 wherein host bus and the plurality of serial buses each comprise a Universal-Serial-Bus (USB), a PCI Express bus, an ExpressCard bus, a Firewire IEEE 1394 bus, a serial ATA bus, or a serial at-

tached small-computer system interface bus.